Amendments to the Drawings:

The attached replacement sheets of formal drawings includes Figs. 1 through 5 and replaces the original sheets including Figs. 1 through 5.

Attachments following last page of this Amendment:

Replacement Sheet (5 pages)

REMARKS

Applicant is re-submitting this amendment to the office action dated January 5, 2005, to respond to the April 6, 2005 examiner's notice of non-compliant amendment. In the April 6, 2005 notice, the examiner indicated that applicant did not properly amend claim 8 with added matter being underlined and deleted matter being stricken through. Applicant has corrected the amendment to claim 8 according to the revised amendment practice document. No new matter was added.

Claims 1-27 are pending in the above-captioned patent application. Claims 1, 10 and 19 are independent claims.

Applicant has enclosed formal drawings to overcome the objections of the official draftsman.

The examiner objected to the title as not being descriptive of the invention.

Applicant disagrees. 37 C.F.R. §1.72(a) states that "the title of the invention, which should be as short and specific as possible, should appear as a heading on the first page of the specification, if it does not otherwise appear at the beginning of the application." Applicant's title is short and specifically points out to the reader that the application involves a local register instruction. Accordingly, applicant believes that the title is complaint with the rules.

The examiner objected to various claims on informal reasons.

Applicant has amended the claims to correct all informalities and to provide proper antecedent basis for all terms with the claims. No new matter was added.

The examiner rejected claims 3-8, 12-17 and 21-26 under 35 U.S.C. §112, first paragraph, as failing the enablement requirement pertaining to the "bit mask."

Applicant amended the detailed description to provide sufficient enablement. No new matter was added. Support for the amendment was contained in the claims as originally filed.

The examiner rejected claims 1-9 as being directed to non-statutory subject matter.

Applicant amended claims 1-9 to recite "A hardware-based multithreaded processor." Support for the amendments is contained in the detailed description as originally filed (see FIG. 3 and related description). No new matter was added.

The examiner uses Hao and Hennessey to reject claim 1-8, 10-17 and 19-26 as having been obvious.

Claim 1 and 19 recite "one of the instructions causing the ALU to load one or more bytes of data within a transfer register associated with one of a plurality of microengines with a shifted value of an operand that preserves the bytes of data that are not loaded," or similar language. Hao and Hennessey neither teach nor suggest this quoted feature, either separately or taken in combination.

The examiner argues that Hao discloses this quoted feature. Applicant disagrees. Hao discloses a set of instructions that utilize the functions of rotation, shifting and merging under a mask and a mechanism for performing the same in a single machine cycle. No preservation of the bytes of data that are not loaded is disclosed or suggested. For example:

> **The processor performs rotate operations on data from a general purpose register (GPR) and returns the result, or a portion of the result, to a general purpose register or to main storage.**
>
> **The rotate operations move a specified number of bits left. The bits that exit from bit position 0 enter at bit position 31 (i.e., a ring shift).**
>
> **The rotate instructions set bits in the Condition Register (CR) according to the value of register RA at the completion of the instruction. The CR is set as if a compare between register RA and the value zero had been performed.**
>
> **The result of the rotate instruction is either inserted into the register under control of the mask provided, or is AND'ed with the mask before being loaded into the register. This operation is effected in the present embodiment by merging (inserting) into a string of all `0`s. (Col. 12, line 55-68, col. 13, lines 1-5)**

No preservation of bytes is taught or suggested.

Hao discloses shift instructions:

> **The instructions of this group logically perform left and right shifts. The result of each instruction is placed in register RA under control of a generated mask. When the mask bit is a 1, the associated bit of the rotated word is placed in register RA. When the mask bit is a 0, the associated bit from either the MQ register, a word of 32 0's, or a word of 32 sign bits from RS is placed in register RA.**
>
> **The shift instructions set bits in the CR according to the value of register RA at the completion of the instruction. The CR is set as if a compare between register RA and the value zero had been performed. (Col. 14, lines 17-28)**

No preservation of bytes is taught or suggested.

Hao discloses rotate and store instructions:

> **The rotate and store instructions allow movement of data from a source field to a destination field where these fields may begin at any address.**
>
> **The result of each instruction is placed in main storage under control of a generated mask. When the mask bit is a 1, the associated bit of the rotated word is placed in main storage. When the mask bit is a 0, the associated bit from the MQ register is placed in main storage. (Col. 18, lines 5-12)**

No preservation of bytes is taught or suggested.

Hennessey fails to make up for at least this deficiency in Hao. Hennessey merely discloses a guide to help readers through a series of worked examples that incrementally add more complex instructions until they have acquired an understanding of the entire MIPS instruction set and the fundamentals of assembly language. No preservation of bytes is taught or suggested. Accordingly, claims 1 and 19 are not rendered obvious by Hao and Hennessey.

Claim 10 recites "clearing the bytes of data that are not loaded."

Neither Hao nor Hennessey teaches, suggests or even mentions clearing the bytes of data that are not loaded. Accordingly, claim 10 is not rendered obvious by Hao and Hennessey.

The examiner uses Hennessey and Kiuchi to reject claims 9, 18 and 27 as having been obvious.

Claims 1, 10 and 19 are not rendered obvious by Hennessey and Kiuchi. Claim 1 and 19 recite ""one of the instructions causing the ALU to load one or more bytes of data within a transfer register associated with one of a plurality of microengines with a shifted value of an operand that preserves the bytes of data that are not loaded," or similar language. Hennessey was discussed above and fails to teach or suggest at least preserving the bytes of data that are not loaded. Kiuchi does not help and merely discloses instruction decoding. For example:

> **The local execution unit (EXU) controller 1750 generates shift control signals provided to the ALU 1712 and the selector 1746 in response to the ALUSHFT signal. The shift control signals received by the selector 1746 control the selector 1746 to provide the shifting code stored by one of the shift registers 1720 or 1722 (sha and shb) to the source B shifter 1752 of the ALU 1712 or to the output shifter 1753 of the ALU 1712. The shift control signal received by the ALU 1712 controls the source B shifter 1752 to shift the source B operand or the ALU output shifter 1753 to shift and round the ALU output by the amount indicated in the shifting code that was provided by the selector 1746. These control signals control the**

ALU 1712 to perform the described shifting functions for those instructions listed in FIGS. 9(a)-(k) that involve bit shifts by with ALU operations. (Col. 41, lines 35-50)

No preservation of bytes is taught or suggested.

As discussed above, Claim 10 recites "clearing the bytes of data that are not loaded."

Neither Hennessey nor Kiuchi teaches, suggests or even mentions clearing the bytes of data that are not loaded.

Claims 9, 18 and 27 depend upon, and add further limitations to, claims 1, 10 and 19. Accordingly, claims 9, 18 and 27 are not rendered obvious by Hennessey and Kiuchi.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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Kenneth F. Kozik
Reg. No. 36,572

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906